

SN54LS31, SN74LS31 DELAY ELEMENTS

SDLS157 – DECEMBER 1983 – REVISED MARCH 1988

- Delay Elements for Generating Delay Lines
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at I_{OL} of 12/24 mA
- PNP Inputs Reduce Fan-In ($I_{IL} = -0.2$ mA MAX)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Ranges

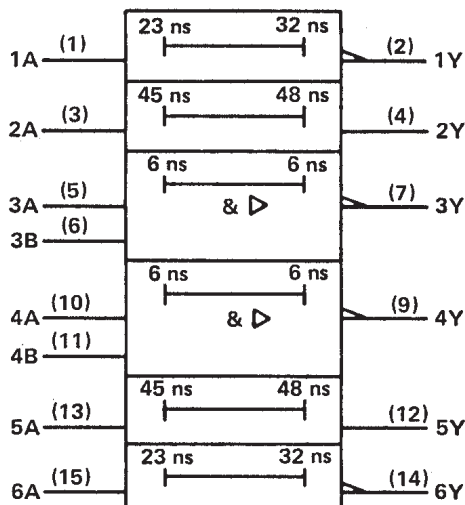
description

These 'LS31 delay elements are intended to provide well-defined delays across both temperature and V_{CC} ranges. Used in cascade, a limitless range of delay gating is possible.

All inputs are PNP with I_{IL} MAX of -0.2 mA. Gates 1, 2, 5, and 6 have standard Low-Power Schottky output sink current capability of 4 and 8 mA I_{OL} . Buffers 3 and 4 are rated at 12 and 24 mA.

The SN54LS31 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS31 is characterized for operation from 0°C to 70°C .

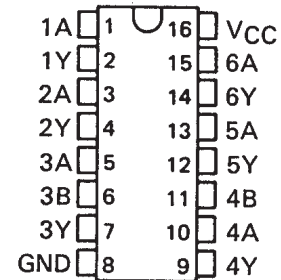
logic symbol†



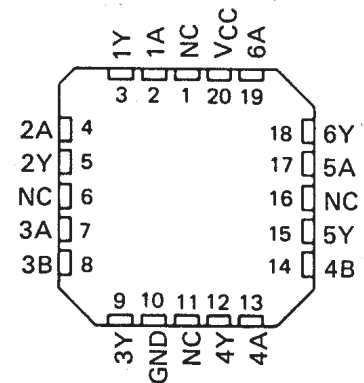
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS31 . . . J OR W PACKAGE
SN74LS31 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS31 . . . FK PACKAGE
(TOP VIEW)

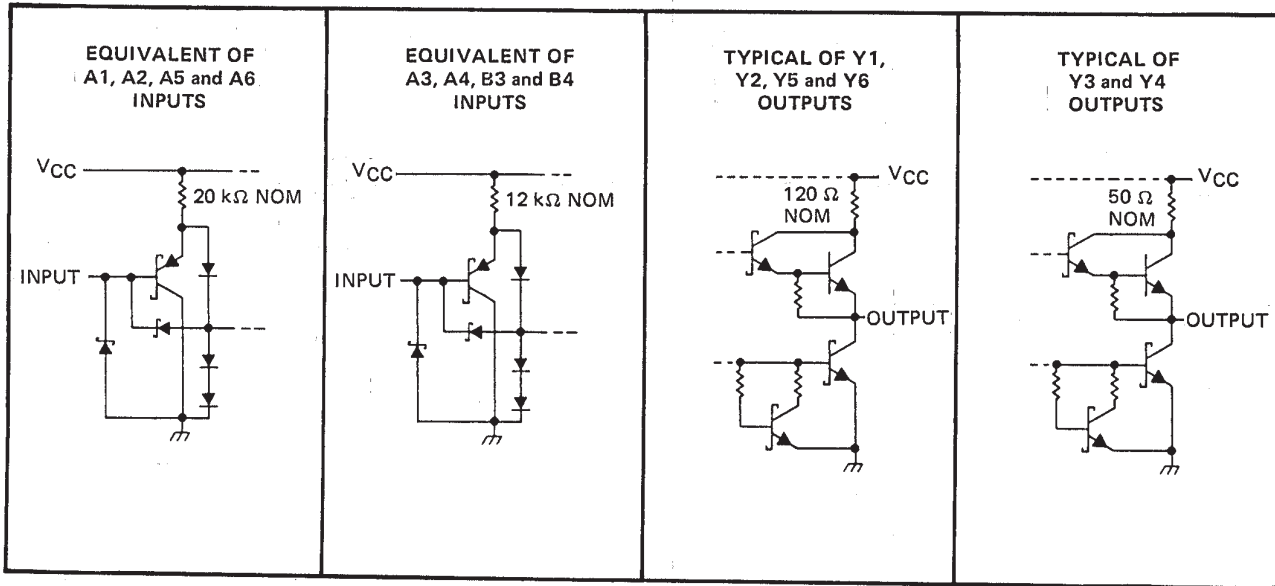


NC - No internal connection

SN54LS31, SN74LS31 DELAY ELEMENTS

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Delay Element	Logic	Typical Delays			Rated I _{OL}
		t _{PLH}	t _{PHL}	AVG.	
Gates 1 and 6	Inverting	32 ns	23 ns	27.5 ns	4 and 8 mA
Gates 2 and 5	Non-Inverting	45 ns	48 ns	46.5 ns	4 and 8 mA
Buffers 3 and 4	2-Input NAND	6 ns	6 ns	6 ns	12 and 24 mA



absolute maximum ratings over operating free air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (See Note 1)	7 V
Input voltage, V _I : All inputs	7 V
Operating free-air temperature range: SN54LS31	– 55°C to 125°C
SN74LS31	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS31			SN74LS31			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current	Y3, Y4 outputs		– 1.2	Y3, Y4 outputs		– 1.2	mA
	All other outputs		– 0.4	All other outputs		– 0.4	
I _{OL} Low-level output current	Y3, Y4 outputs		12	Y3, Y4 outputs		24	mA
	All other outputs		4	All other outputs		8	
T _A Operating free-air temperature	– 55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS31			SN74LS31			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5			V	
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	Y3, Y4	I _{OH} = -1.2 mA			2.4 3.1			V	
		Others	I _{OH} = -0.4 mA			2.5 3.1				
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	Y3, Y4	I _{OL} = 12 mA			0.25 0.4			V	
			I _{OL} = 24 mA			0.35 0.5				
		Others	I _{OL} = 4 mA			0.25 0.4				
			I _{OL} = 8 mA			0.35 0.5				
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1			mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20			μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.2			-0.2			mA	
I _{OS} §	V _{CC} = MAX, A3, A4, B3, B4 = 0 V		Y3, Y4			-30 -130			mA	
	V _{CC} = MAX, A1, A6 = 0 V, A2, A5 = 4.5 V		Y1, Y2, Y5, Y6			-20 -100				
I _{CC}	I _{CC} H	V _{CC} = MAX, A2, A5 = 4.5 V, all other inputs 0 V		2.3 4			2.3 4			mA
	I _{CC} L	V _{CC} = MAX, A2, A5 = 0 V, all other inputs 4.5 V		13 20			13 20			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LS31			SN74LS31			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	A1, A6	Y1, Y6	15			22			ns
t _{PHL}			70			65			
t _{PLH}	A2, A5	Y2, Y5	9			13			ns
t _{PHL}			50			45			
t _{PLH}	A3, B3, A4, Y4	Y3, Y4	22			31			ns
t _{PHL}			90			80			
t _{PLH}	Y4	Y3, Y4	20			30			ns
t _{PHL}			105			95			
t _{PLH}	Y4	Y3, Y4	2			2			ns
t _{PHL}			20			15			
t _{PHL}	Y4	Y3, Y4	2			2			ns
t _{PHL}			20			15			

NOTE 2: V_{CC} = MIN to MAX

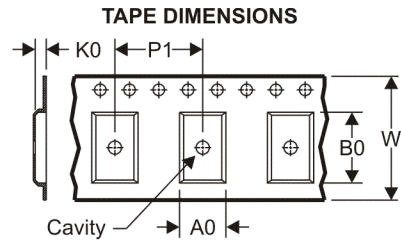
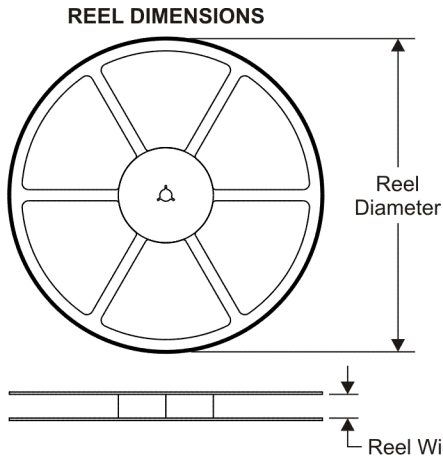
R_L = 667 Ω, C_L = 45 pF for Y3 and Y4.

R_L = 2 kΩ, C_L = 15 pF for Y1, Y2, Y5 and Y6.

T_A = MIN to MAX

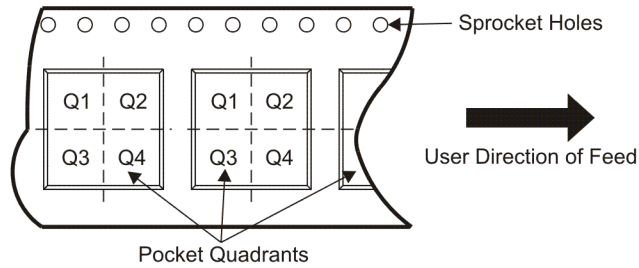
Load circuits and voltage waveforms are shown in Section 1.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

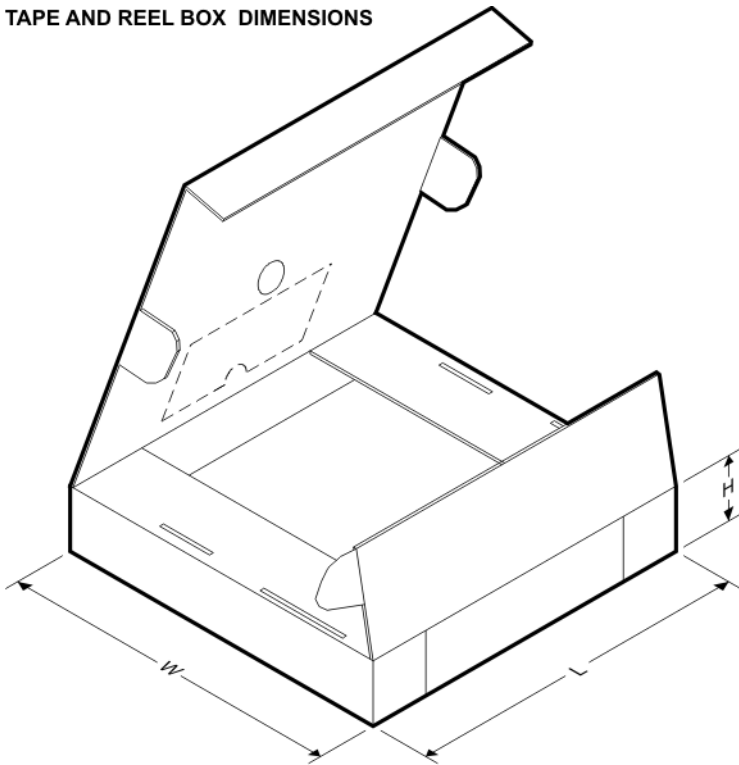
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS31DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS31NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS31DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS31NSR	SO	NS	16	2000	346.0	346.0	33.0

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